REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-17 remain under consideration. Claims 18-26 have been withdrawn from consideration as being drawn to a non-elected species. The Examiner is respectfully requested to reconsider his rejections in view of the amendments and remarks as set forth below.

OBJECTION TO THE DRAWINGS

The drawings stand objected under 37 C.F.R. §1.83(a). In particular, the Examiner requires that the recitation in claim 6 of the substrate-triggered MOS connected to first and second power lines must be shown. Applicants submit that this feature is already in the figures, namely Figs. 6 and 12. First, in Fig. 6 on the left-hand side of the figure there is an N-type substrate-triggered MOS indicated as MESD. One of the terminals in this NMOS is connected to power line VDDA and the other is connected to power line VSSA. This is also seen in Fig. 12, where this device has connections to source 62 and drain 60. These contacts are connected to VDDA and VSSA as shown in Fig. 6. During an ESD event with a positive pulse on pad 30 and VSSA grounded, the substrate 58 of MESD will be biased with a current from VSSD to trigger the parasitic bipolar junction transistor under MESD. Thus, Applicants submit that the features of claim 6 are shown in Figs. 6 and 12 and that no change to the drawings is necessary.

Rejection under U.S.C. §112

Claims 8-15 stand rejected under 35 U.S.C. §112, as being indefinite. This rejection is respectfully traversed.

With regard to claim 8, the Examiner objects to the "second bias voltage" sensor as having no basis for a "first bias voltage". By way of the present amendment, the word "second" has been removed from claim 8. Likewise, claim 7 has been amended to remove the word "first" so that each claim only refers to a biased voltage. Since these claims do not depend from each other and no claims depend from either of these claims, this language is now considered to be definite.

With regard to claim 15, the Examiner felt that the term "another source/drain" was vague. By way of the present amendment, Applicants have amended claim 13 from which claim 15 depends to recite a first source/drain and claim 15 has been amended to now refer to "a second source/drain". Thus, all of the rejections under 35 U.S.C. § 112, are now believed to be overcome.

Rejection under 35 U.S.C. § 102

Claims 1, 3, 14, 16 and 17 stand rejected under 35 U.S.C. § 102 as being anticipated by Jun et al. (U.S. Patent No. 6,406,948). This rejection is respectfully traversed.

The Examiner states that the Jun reference shows an ESD protection circuit suitable for an I/O pad and a plurality of diodes as shown in Fig. 10, stacked and coupled between the first power line and the pad. The Examiner also states that during normal operation the diodes are reverse-biased, and, when an ESD event occurs between a

second power line and the pad, the diodes are forward-biased to conduct the ESD current.

Claim 1 describes an electro-static discharge protection circuit for low input capacitance for an I/O pad, having a combination of elements including a plurality of diodes stacked and coupled between a power line and the I/O pad. The diodes are reverse biased in normal operation and when an ESD event occurs between a second power line and the pad, the diodes are forward biased to conduct an ESD current.

Applicants disagree with the Examiner's understanding of the Jun reference. The Examiner relies on Fig. 10 of Jun to show a plurality of stacked diodes. Applicants believe that while this figure initially seems to indicate that the diodes are stacked, in fact there are no stacked diodes in this reference. There is essentially no description of Fig. 10 itself except in the Brief Description at column 2, lines 31 and 32 and the short paragraph of column 3, lines 57-59. This paragraph merely states that the areas shown relate to the schematic of Fig. 9. There is no brief description of the diodes being stacked in regard to any of the figures of the reference. The complete description of the diodes is found at column 3, lines 45-55. The diodes are described as being large area diodes which do not impose a restriction on the silicon real estate. Higher voltages can be withstood by this design and then may be 2 μm by 2 μm up to hundreds of μm in area. This description of the diodes does not in any way describe them as being stacked. As will be pointed out later, in fact the description seems to indicate that these should not be stacked.

Further, this description of the diodes does not in any manner indicate that the diodes are reverse biased during normal operation and forward biased when an ESD event occurs. Further, the description does not describe the circuit as having a low input capacitance as described in the claim. Because the description of the Jun reference does not show these features, Applicants submit that claim 1 should not be rejected thereover.

Further, in regard to the question of whether the diodes are stacked, it is noted that in Fig. 10, ellipses are formed at 4 points with reference numerals indicating areas 10, 12, 14 and 16 in Fig. 9. Therefore, one set of diodes is formed between substrate 10 and N^+ region 14. Since these two regions are adjacent, and of opposite conductivity type, it would appear that a single diode would be involved. Likewise, N well 12 and P^+ region 16 are likewise adjacent and of opposite conductivity so that a single diode would also be appropriate between the ellipses in Fig. 10 regarding this. Thus, it would appear that stacked diodes would be inappropriate.

As a more full explanation, reference is made to an attached copy of Fig. 9 of the reference, with markings being added for clarity. In this figure, the source/drain regions 32 and the wells which are formed thereunder are marked. The source drain regions on the left side are indicated as 32L and those on the right side as 32R. The well under the regions 32L is indicated by 39L while the well under 32R is indicated as 39R. As indicated in the specification, layer 18 is silicon oxide as is layer 24. The silicon substrate 10 is P-type.

If well 39R is P-type silicon, it will provide a DC short path between P^+ region 16 and P substrate 10. In Fig. 10, P^+ 16 and P substrate 10 must be separated by diodes. Therefore, well 39R must be N-type silicon and source/drain 32R must be P-type silicon to form a PMOS.

In Fig. 9, if the MOS on the left is the same type as the MOS on the right side, the inventor need not show there are different connection structures. Therefore, one would conclude that the MOS on the left is a NMOS with N-type source/drain regions 32L and a P-type well 39L.

These conductivity types are marked in the respective regions in the attached drawing. In addition, possible diodes in Fig. 9 have been added with diode D1 formed between N^+ region 14 and P substrate 10, diode D2 between N^+ region 14 and P well 39L, diode D3 between P well 39L and N source/drain region 32L, diode D4 between P substrate 10 and N well 12, diode D5 between P regions 16 and N well 12 and diode D6 between P source/drain region 32R and N well 39R.

The equivalent diodes between N region 14 and P substrate 10 are diodes D1, D2 and D3 but all of these diodes are connected in parallel and not in series as shown in Fig. 10. The equivalent diodes between P region 16 and N well 12 are diodes D4, D5 and D6 and these diodes are connected in parallel and not in series as shown in Fig. 10. Thus, given this information, it is clear that there are no stacked diodes in Fig. 9, contrary to the drawing of Fig. 10. Thus, one skilled in the art would know that the manner of drawing Fig. 10 is actually

incorrect and that each diode string should be replaced with a single diode according the description in the specification of Fig. 9. Given this, it is clear that the Jun reference does not provide the stacked diodes and accordingly, claim 1 is allowable thereover.

Claims 2-17 depend from claim 1 and as such are also considered to be allowable. In regard to claim 2, it is noted that claim requires a doped area in a first well and a deep well formed under the first well. The Examiner has referred to region 16 and well 12 but has not shown that the reference includes a deep well under the first well. Thus, Applicants submit that claim 2 is further allowable.

Claim 3 also describes that the first well is surrounded by a second well. This relates to N well 56 shown in Fig. 12, for example. This is not described anywhere in the Jun reference.

Claim 6 not only describes the clamp circuit but specifically describes the substrate-triggered MOS and its connections. This is not described in any manner in the Jun reference.

Claim 9 also refers to the deep well which is not seen in this reference. Claim 10 likewise relates the second well in a similar fashion to claim 3.

In regard to claim 13, the Examiner states that Jun shows a diode formed by a PN junction between a source/drain and a substrate. This is not seen. If the Examiner persists in this, he is requested to point out where this is located.

Rejection under 35 U.S.C. §103

Claims 2-4 stand rejected under 35 U.S.C. §103(a) as being obvious over Jun. Applicants further submit that either adding a doped area to the first area or adding a deep well under the first well would not be obvious since there is no indication of the need to do so in this reference. The Examiner is requested to provide an indication of why one skilled in the art would be motivated to make this change if he persists in this rejection.

Claims 3 and 4 depend from claim 2 and are further allowable based on this dependency as well.

Claims 5-12 and 15 stand rejected as being obvious over Jun in view of Watt (U.S. Patent No. 5,623,156). The Examiner cites the Watt reference to show an ESD with a clamp circuit. First, Applicants submit that it would not be obvious to combine these two references. The Examiner indicates no motivation for one skilled in the art to use this clamp circuit in Jun. Jun does not teach the need to have such a circuit and there is no need to add one to the functioning device of Jun. Further, it is submitted that it would not be obvious to include a substrate-triggered MOS with the substrate node biased with suitable current to trigger a bipolar junction transistor parasitizing and conducting ESD current when an ESD event occurs.

Furthermore, in regard to claim 9, the Examiner admits that the combination of references does not teach an MOS formed in a first well surrounded by a second well. Applicants submit that it would not be obvious to one skilled in the art to modify this combination of

references to teach this concept. Again, Applicants do not see any motivation to do this. Likewise, in regard to claim 10 it would not be obvious to surround the first well with the second well.

The remaining claims are also allowable based on their dependency from the allowable independent claims.

CONCLUSION

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner either alone or in combination. In view of this, reconsideration of the rejections and allowance of all of the claims are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert Gnuse (Reg. No. 27,295) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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0941-0316P

Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

7. (Amended) The ESD protection circuit as claimed in claim 6, wherein the substrate-triggered MOS includes a gate applied with a [first] bias voltage to keep the substrate-triggered MOS off during normal operations.

8. (Amended) The EDS protection circuit as claimed in claim 6, wherein the gate is applied with a [second] bias voltage to speed up the turn-on rate of the substrate-triggered MOS when an ESD event occurs.

13. (Amended) The ESD protection circuit as claimed in claim 1, wherein the diode includes a PN junction diode formed by a PN junction between a first source/drain and a substrate of a MOS.

15. The ESD protection circuit as claimed in claim 13, wherein the gate of said MOS is coupled to [another] a second source/drain of the MOS.

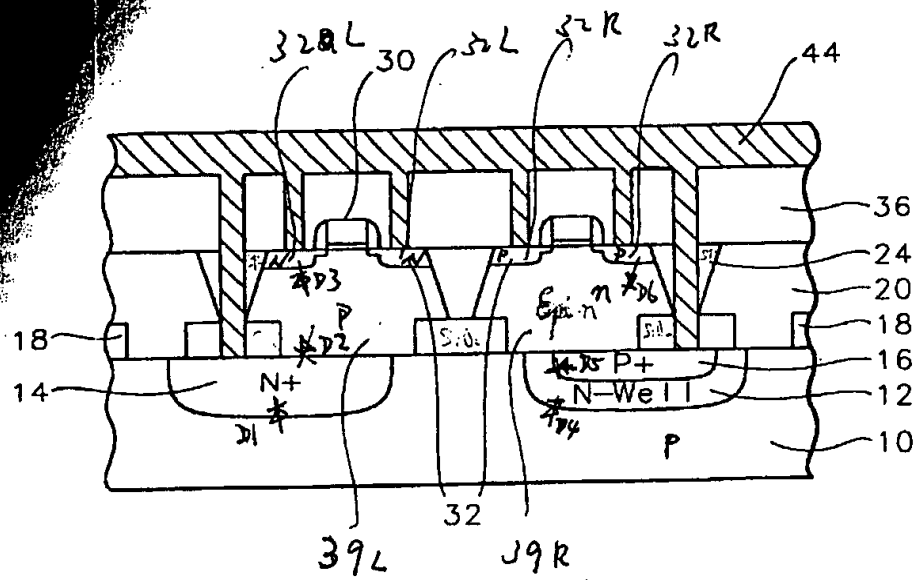

FIG. 9

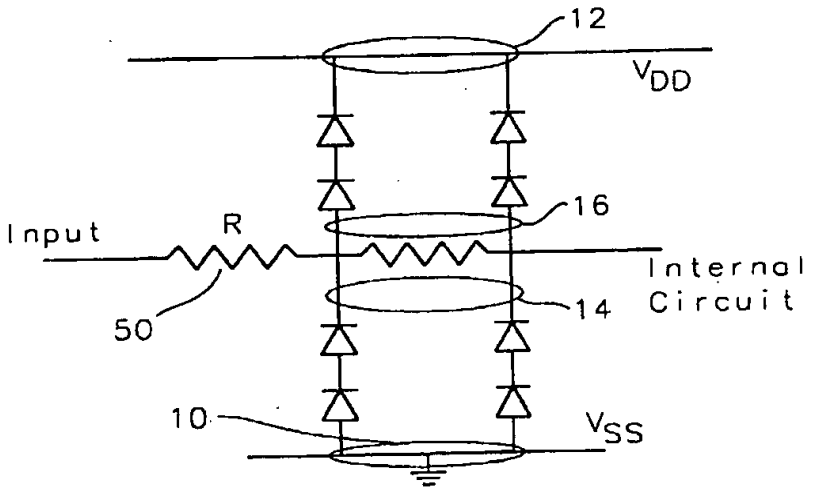

FIG. 10